

The diagram illustrates a digital signal processor (DSP) system. The central component is a DSP (10). It is connected to a ROM (12) and a RAM (14). The DSP (10) has an internal bus structure with multiple lines connecting to the ROM (12) and RAM (14). The RAM (14) is further connected to a set of external buses labeled PRAB, PRDB, DRAB, DRDB, DWAB, and DWDB. The DSP (10) also has an 'Int' (interrupt) line connected to a Logic interface (26). The Logic interface (26) is connected to a Scan-path interface (18) and a Switching circuit (24). The Scan-path interface (18) is connected to the DSP (10) and the Switching circuit (24). The Switching circuit (24) is connected to a Host interface (20) and a Universally used I/O (22). The Host interface (20) and the Universally used I/O (22) are connected to external buses labeled LAB, LDB, and LCB. The entire system is enclosed in a box labeled 16, with various input/output lines extending from the bottom.

19

24

To the scan-path interface circuit (18)

Gate circuit

36

To the terminal pin for the emulation

20

24

LDB

38

Register

Gate circuit

36

To the scan-path interface circuit (18)

To the terminal pin for the emulation

21

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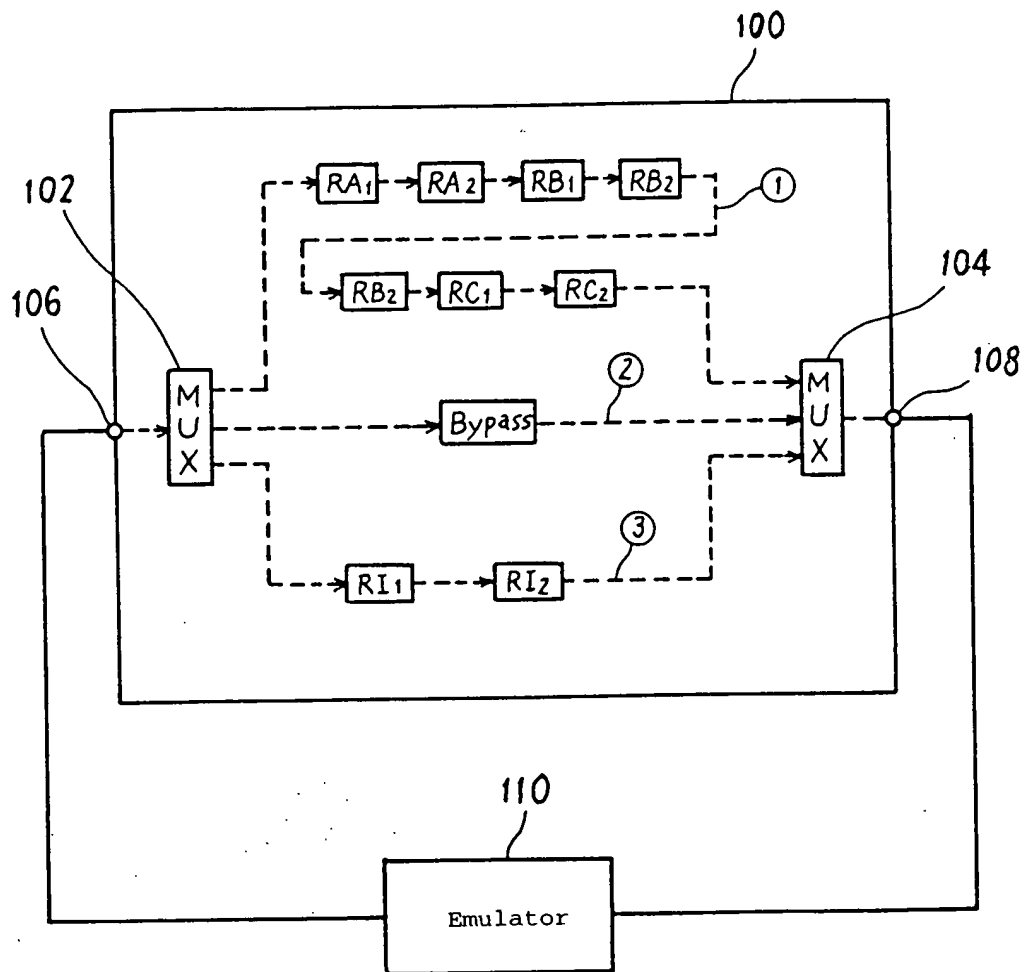


FIG. 4